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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/078,180	02/19/2002	Neil G. Morrow	TI-31574	5454

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EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 07/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/078,180	MORROW, NEIL G.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8 and 15-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8 and 15-17* is/are rejected.

7)☒ Claim(s) *8 and 15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art ("AAPA") and US Patent Number 6,070,214 to Ahern ("Ahern").

3. In reference to Claim 8, AAPA teaches a bus repeater comprising a first portion connected to a first segment of a host bus and a second portion connected to a second, non-hierarchical segment of the host bus, wherein the first portion further comprises an interface to the first bus segment (See Page 2 Lines 3-11). AAPA further teaches a link translation layer further comprising a transaction decode circuit connected to the interface to the first bus segment to determine by subtractive decode which transactions on the first bus segment to accept and pass on to the second bus segment (See Page 2 Lines 5-6). AAPA does not teach that the first and second portions of the repeater are located remotely and are connected by a serial link, and a transaction queue with a data

buffer connected to the interface. Ahern teaches using a serial link to connect two remotely located bus interfaces (See Figures 2 and 5 Numbers 40 and 46, Column 7 Lines 21-33, and Column 9 Lines 19-24) and a transaction queue with a data buffer connected to the interface (See Figure 1 Number 18 and Column 5 Line 66 – Column 6 Line 8).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the repeater of AAPA with the serial link allowing the portions of the repeater, and thus the bus segments, to be located remotely of Ahern, resulting in the invention of Claim 8, in order to allow the bus to be extended over longer distances without the need for a large cable with high latency (See Column 2 Lines 18-22 of Ahern and Page 2 Lines 17-22 of AAPA), and because the repeater of AAPA and the bridge of Ahern perform similar functions, and one would naturally look to bus bridges when constructing a bus repeater.

4. In reference to Claim 16, AAPA and Ahern teach the limitations as applied to Claim 8 above. Ahern further teaches that the host bus is a PCI bus (See Column 1 Lines 51-65).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the repeater of AAPA with the serial link allowing the portions of the repeater, and thus the bus segments, to be located remotely of Ahern, resulting in the invention of Claim 16, in order to allow the bus to be extended over longer distances without the need for a large cable with high latency (See Column 2

Lines 18-22 of Ahern and Page 2 Lines 17-22 of AAPA), and because the repeater of AAPA and the bridge of Ahern perform similar functions, and one would naturally look to bus bridges when constructing a bus repeater.

5. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA and Ahern as applied to Claim 8 above, and further in view of "IEEE Standard for a High Performance Serial Bus" ("IEEE-1394").

6. In reference to Claim 15, AAPA and Ahern teach the limitations as applied to Claim 8 above. AAPA and Ahern do not teach that the serial link is one of LVDS, Gigabit Ethernet, InfiniBand, IEEE 1394, RF Wireless, or Infrared Wireless. IEEE-1394 teaches the use of an IEEE 1394 bus as a serial bus.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of AAPA and Ahern using an IEEE 1394 bus as the serial bus, resulting in the invention of Claim 15, because the IEEE 1394 serial bus is a powerful and low-cost interconnect allowing bandwidths comparable with existing I/O interconnect standards and is architecturally compatible with parallel computer buses which leads to lower communication function overhead (See Page 3 Section 1.4.2 and Page 1 Section 1.1 of IEEE-1394).

7. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Ahern, and IEEE-1394 as applied to Claim 15 above, and further in view of "Low Pin Count Interface Specification" by Intel ("Intel 1997").

8. In reference to Claim 17, AAPA, Ahern, and IEEE-1394 teach the limitations as applied to Claim 15 above. AAAP, Ahern, and IEEE-1394 do not teach that the host bus is an LPC bus as defined by Intel 1997. Intel 1997 teaches the use of a serialized LPC bus (See Page 1 Chapter 1 and Page 6 Section 4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a construct the device of AAPA, Ahern, and IEEE-1394 using the LPC buses of Intel 1997, resulting in the invention of Claim 17, because LPC has a reduced cost, allows synchronous design, is transparent and thus does not require special drivers or configuration, and supports desktop and mobile implementations (See Page 1 Section 1.1 of Intel 1997).

9. Claims 8 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Application Publication Number 2002/0072357 to Matsuda ("Matsuda") and US Patent Number 5,568,619 to Blackledge et al. ("Blackledge").

10. In reference to Claim 8, Matsuda teaches a first repeater portion (See Figure 2 Number 15) connected to a first segment of the host bus (See Figure 2 Number 17c); a second repeater portion (See Figure 2 Number 16) connected to a second, non-

hierarchical segment of the host bus remote from the first segment of the host bus (See Figure 2 Number 18c), where the first and second portions of the repeater are connected by a serial link (See Figure 2 Number 110), wherein at least one of the repeater portions further comprises: an interface to the first bus segment (See Figure 3 Number 27); a transaction queue with a data buffer connected to the interface (See Figure 3 Number 20); and a link translation layer connected to the transaction queue to translate incoming transactions from the first bus segment into serial streams to be sent over the serial link (See Figure 3 Number 20 and Page 4 Paragraph 58). Matsuda does not teach determining by subtractive decode which transactions on the first bus segment to accept and pass on over the serial link. Blackledge teaches the use of subtractive decoding in bus interfaces (See Column 2 Lines 8-25).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to construct the device of Matsuda using the subtractive decoding of Blackledge, resulting in the invention of Claim 8, because subtractive decoding requires minimum hardware circuitry (See Column 2 Lines 12-13 of Blackledge) because the repeater of Matsuda and the bridge of Blackledge perform similar functions, and one would naturally look to bus bridges when constructing a bus repeater.

11. In reference to Claim 15, Matsuda and Blackledge teach the limitations as applied to Claim 8 above. Matsuda further teaches that the serial link is RF wireless (See Figure 2 Number 110 and Pages 3-4 Paragraph 55).

It would have been obvious to one or ordinary skill in the art at the time the invention was made to construct the device of Matsuda using the subtractive decoding of Blackledge, resulting in the invention of Claim 15, because subtractive decoding requires minimum hardware circuitry (See Column 2 Lines 12-13 of Blackledge) because the repeater of Matsuda and the bridge of Blackledge perform similar functions, and one would naturally look to bus bridges when constructing a bus repeater.

12. In reference to Claim 16, Matsuda and Blackledge teach the limitations as applied to Claim 8 above. Blackledge further teaches a bus interface for coupling to a PCI bus.

It would have been obvious to one or ordinary skill in the art at the time the invention was made to construct the device of Matsuda using the subtractive decoding and PCI host bus of Blackledge, resulting in the invention of Claim 16, because subtractive decoding requires minimum hardware circuitry (See Column 2 Lines 12-13 of Blackledge); because PCI is a widely accepted bus standard which is capable of performing significant data transfer in a relatively short period of time (See Column 1 Lines 21-41 of Blackledge); and because the repeater of Matsuda and the bridge of Blackledge perform similar functions, and one would naturally look to bus bridges when constructing a bus repeater.

13. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda and Blackledge as applied to Claim 15 above, and further in view of Intel 1997.

14. In reference to Claim 17, Matsuda and Blackledge teach the limitations as applied to Claim 15 above. Matsuda and Blackledge do not teach that the host bus is an LPC bus as defined by Intel 1997. Intel 1997 teaches the use of a serialized LPC bus (See Page 1 Chapter 1 and Page 6 Section 4.2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a construct the device of Matsuda and Blackledge using the LPC buses of Intel 1997, resulting in the invention of Claim 17, because LPC has a reduced cost, allows synchronous design, is transparent and thus does not require special drivers or configuration, and supports desktop and mobile implementations (See Page 1 Section 1.1 of Intel 1997).

Claim Objections

15. Claims 8 and 15-17 are objected to because of the following informalities: In Line 10 of Claim 8, the word "to" appears to have been omitted from between the words "connected" and "the". Appropriate correction is required.

Response to Arguments

16. Applicant's arguments with respect to Claims 8 and 15-17 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

17. The following prior art made of record and not relied upon is considered pertinent to Applicant's disclosure: US Patent Number 5,734,850 to Kenny et al. and "Intel 380FB PCISET: 82380FB MOBILE Docking Controller (MPCI2)".

18. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 571-272-3624. The Examiner can normally be reached on Monday-Thursday (7-3:30), Alt. Fridays (7-2:30).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

Khanh Dang
Primary Examiner

Thomas J. Cleary
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Art Unit 2111